Remarks

The present response is to the Office Action mailed the above-referenced case on September 10, 2007. Claims 1-11, 13-25, 27 and 28 are standing for examination.

Merit rejection under 35 U.S.C. 103(a)

Claims 1, 2, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Atsmon et al (US Patent #6,607,136) hereinafter Atsmon, in view of Leydier et al (PG Pub #US 2003/0046554 A1) hereinafter Leydier.

Examiner's rejection

9. Regarding claim 15, Atsmon discloses a secure memory device (system shown in figure 1) for use with and contained within a smart card with a modem interface comprising circuitry of:

A rewritable memory (memory unit 22, figure 2; column 12, lines 38-42);

A processing unit or a microprocessor (processing unit 21);

An on-chip oscillator (oscillator circuit or RC circuit; column 13, lines 4-11), circuitry of which is contained in the secure memory device; examiner notes that Atsmon teaches both circuits being external. However, both circuits are external to the processor, not to the card. This is evidenced by the fact that Atsmon teaches the type of oscillator used is limited by the size of the card. Atsmon also teaches that the oscillator would be connected to the OSCIICLKIN pin of the processor (figure 7). Accordingly, examiner asserts that the oscillator is on-chip (on the card).

An IS0 7816 interface (column 25, lines 12, 13);

A one-wire modem interface (transducer; column 11 , lines 37-39);

Characterized in that both communication interfaces are bidirectional (input/output unit 35, figure 3; column 11, lines 36-40); Examiner notes that the I/O unit 35 can both receive and transmit data (therefore bi-directional).

Atsmon does not disclose explicitly that both communication interfaces share the same I/O terminal. However, Leydier discloses a smartcard (figure 13) such that communication interfaces (ISO, USB, Wireless ports) share a single I/O terminal (communication interface 190, paragraph 59) providing a single connection port on the secure memory device for both of the communication devices (figure 13, connection port to processor 169). Teachings of Atsmon and Leydier are from the same field of smartcards, and specifically of multiple communication interface smartcards.

Therefore, it would have been obvious at the time of invention for a person of ordinary skill in the art to combine teachings of Atsmon and Leydier by using a common I10 terminal in the smartcard system of Atsmon for the benefit of converting data between different protocols (paragraph 59).

Applicant's response

Applicant argues that Atsmon fails to teach that the oscillator is on-chip, as claimed. The Examiner states; "Atsmon teaches both circuits being external. However, both circuits are external to the processor, not to the card. This is evidenced by the fact that Atsmon teaches the type of oscillator used is limited by the size of the card. Atsmon also teaches that the oscillator would be connected to the OSCIICLKIN pin of the processor (figure 7). Accordingly, examiner asserts that the oscillator is on-chip (on the card)."

Applicant points out, as known in the art of electronics, an integrated circuit (also known as IC, microcircuit, microchip, silicon chip, or chip) is a miniaturized electronic circuit (consisting mainly of semiconductor devices, as well as passive components) that has been manufactured in the surface of a thin substrate of semiconductor material. A smart card, chip card, or integrated circuit card (ICC), as disclosed in Atsmon, is known in the art as any pocket-sized card with embedded integrated circuits which can process information.

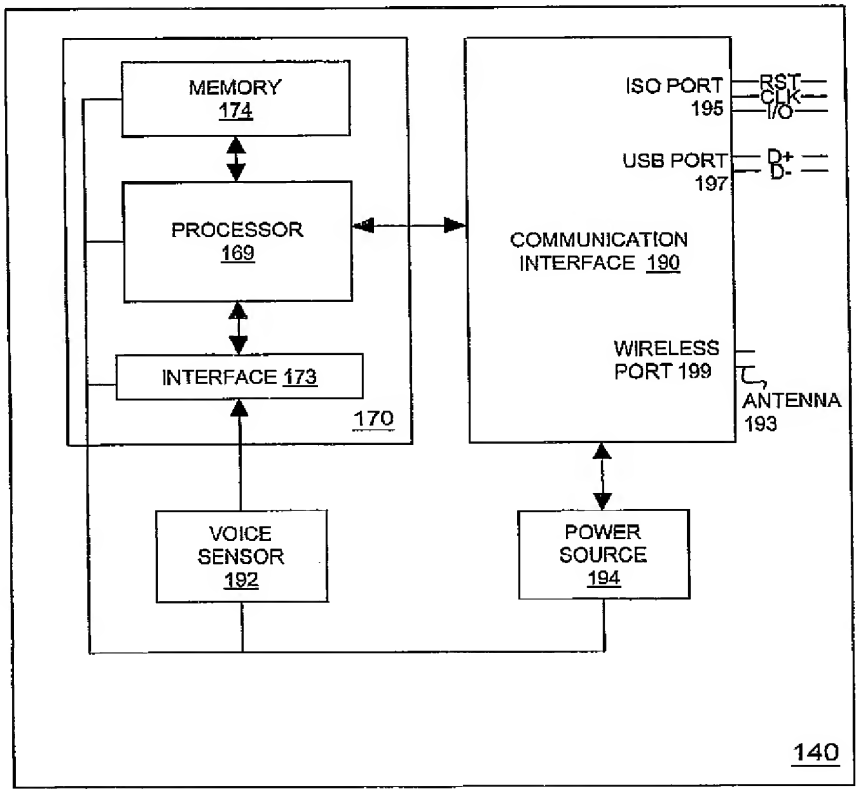
As demonstrated above, a chip and a card, as known in the art are not identical, as espoused by the Examiner. Applicant claims an on-chip oscillator. Atsmon clearly teaches that an oscillator is in the card, which is not necessarily on-chip, as argued above.

The Examiner states Atsmon teaches; "Characterized in that both communication interfaces are bidirectional (input/output unit 35, figure 3; column 11, lines 36-40); Examiner notes that the I/O unit 35 can both receive and transmit data (therefore bi-directional);

Atsmon does not disclose explicitly that both communication interfaces share the same I/O terminal. However, Leydier discloses a smartcard (figure 13) such that communication interfaces (ISO, USB, Wireless ports) share a single I/O terminal (communication interface 190, paragraph 59) providing a single connection port on the secure memory device for both of the communication devices (figure 13, connection port to processor 169). Teachings of Atsmon and Leydier are from the same field of smartcards, and specifically of multiple communication interface smartcards.

Applicant points out that claims 1 and 15 actually read; "*characterized in that both communication interfaces are bidirectional and share a single I/0 terminal providing a single connection port on the secure memory device for both of the communication interfaces.*"

Figure 13 of Leydier is reproduced below. The Examiner relies upon the arrow between communication interface 190 and processor 169 to read on a single connection port, as claimed.



Applicant believes the Examiner may be assuming subject matter or adding subject matter to the art of Leydier when relying on the reference to reject applicant's said claim limitation. Leydier does not disclose in detail the type of connection the arrow portrays between communication interface 190 and processor 169. Applicant argues that Leydier's figure and accompanying text fail to support the Examiner's statement that; "communication interfaces (ISO, USB, Wireless ports) share a single I/O terminal (communication interface 190, paragraph 59) providing a single connection port on the secure memory device for both of the communication devices (figure 13, connection port to processor 169)."

Applicant's claim specifically reads "a single I/0 terminal providing a single connection port on the secure memory device for both of the communication interfaces." Leydier's I/O terminal is part of the ISO port, therefore Leydier fails to teach what the Examiner espouses, specifically "a single I/O port providing a single connection port for both devices.

Applicant argues that the art of Atsmon and Leydier cannot be combined as stated by the Examiner because there is still no single communication port capability shown in the art, as claimed in applicant's invention.

Independent claims 15, as argued, is clearly patentable over the art presented by the Examiner, as argued above. Claim 1 includes similar limitations as argued for 15 and is patentable relying on the same reasoning provided by applicant, above. Dependent claims 2-11, 13-14, 16-25, and 27-28 are patentable on their own merits, or at least as dependent upon a patentable base claim.

As all of the claims standing for examination have been shown to be patentable over the art of record, applicant respectfully requests reconsideration, and that the present case be passed quickly to issue. If there are any time extensions needed beyond any extension specifically requested with this response, such extension of time is hereby requested. If there are any fees due beyond any fees paid with this amendment, authorization is given to deduct such fees from deposit account 50-0534.

Respectfully Submitted,
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